

UWB PMC/XMC I/O Module

2 Ch. Ultra-Wide-Band Receiver
210MSPS A/D's
Large FPGA for User Code
Deep memory



Features

- Two LTC2220-1, 12-bit 210 MSPS converters
- Virtex-II Pro FPGA, 4 Million gates
- PCI 64/66 with Pn4 port to host card
- XMC - 1GB/s full duplex rates per VITA 42
- 64MB SDRAM plus 2MB RAM for FPGA
- Sample clocks: dual external or on-card PLL
- Advanced SW and firmware demo programs
- External Trigger control
- Full FPGA development system (VHDL or MatLab/Simulink)
- Supported by MatLab/Simulink

Applications

- Software Defined Radio (SDR)
- Signal Identification
- Electronic Warfare
- Advanced RADAR
- Hardware Testing
- Telecom IP development



Ordering Information

UWB PMC Module	80144-2
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Overview

The UWB Receiver PMC/XMC card features the most advanced architecture for ultra-fast signal capture and real-time processing in wide-band radio systems and similar wide spectrum applications. It integrates two 210 MSPS, 12-bit A/D channels with a large FPGA for user-code, ample memory and flexible clocks/triggers on a PMC/XMC mezzanine format. The UWB has Xilinx VirtexII Pro FPGA for signal processing that may be quickly customized using Innovative's Framework Logic in VHDL or in the MATLAB Simulink graphical environment. Large on-card memories for data capture and analysis, a flexible clocking structure, and 1GB/s connectivity to host DSP cards make the UWB a powerful front end to many applications. This interface offers a very high-rate, low latency connection to Innovative Integration's Velocia series of DSP and FPGA compactPCI boards and this port protocol can be reconfigured in logic to communicate with third party host cards.

Description

The UWB Receiver PMC card is a two-channel ultra-wide-band digital receiver with advanced architecture that provides ultimate flexibility and speed for the most advanced RF signal capture and hardware-assisted signal processing.

The front-end features two analog input channels consisting of a 50-ohm single-ended input followed by Linear Technology's LTC2220-1 converter. The A/D data flows directly to the FPGA for processing. The sample rate clock may be selected from one of two external clock inputs or from the on-card PLL. The external clocks may be used directly as a sample clock or divided down and used as a PLL reference. The on-board PLL timebase provides a low-jitter, flexible conversion clock that is programmable by the FPGA. The on-board time base is a highly accurate PLL device ranging from 31MHz to 700MHz with a 5 pico-second maximum RMS jitter. Alternatively, the user can provide individual external clock for each channel, using 50 Ohm SMB inputs. The external clock may be used as a PLL reference.

The UWB Receiver PMC card shares a common architecture with numerous other VelociaPMC cards. This include a large user-FPGA with dedicated SBSRAM, a PCI-FPGA with large global RAM and private port over PMC connector J4 to the select host cards, such as Innovative Integration's Velocia family. The XMC connection to the host card, with four 2.5Gbps full duplex lanes, provides 1GB per second connectivity.

The PCI interface is a packet protocol system that provides up to 528MB/sec performance over a 64-bit capable PCI bus, yet allows the flexibility of on-demand, channel based data control. This packet protocol system allows the system developer to easily integrate the PMC into the system by delivering on-demand channelized data to applications and integrate custom data packets and streams into the data flow. A secondary lower speed command and control channel over the PCI bus complements the packet system for status and control functions to the application logic.

Ample logic resources allow for flexible integration of the most demanding signal processing blocks such as down/up conversion, complex filtering, resampling, spreading/despreading and clock recovery. For example, the Xilinx DDC logic core for GSM consumes only about 2% of the logic and 1 multiplier. (VP30 and VP50 can be offered as options)

The application-FPGA controls the I/O, the PLL time base, triggers, 64MB of DDR SDRAM for large data buffering, and a dedicated 2MB SBSRAM. The large 64MB DDR SDRAM memory is

System Generator may be used for logic development. This powerful tool set allows the signal processing designer to develop algorithms using all the power and grace of MATLAB and then implement them directly in logic. The Framework Logic provides blocks for the hardware interface ready to use in the Simulink graphical design environment. Gateways to MATLAB allow the developer to quickly test the system by using Simulink to generate, analyze and display the actual data on the hardware during design. Nothing could be easier for advanced signal processing development!

The PCI-FPGA is not intended for end-user logic development and source code is usually not provided. Contact Innovative Integration if your application might require changes to these specific interfaces.

Software Support

Innovative Integration's software tool kit for the VelociaPMC series is a powerful collection of software libraries, utilities, examples projects and interactive help file that allow developers to be very productive from the start. Numerous program examples - with source code- demonstrate the usage of every peripheral on the board and provide a framework for further custom development.

OEM Configurations

The UWB VelociaPMC board can be configured or modified to fit your specific requirements and provide an optimal mix of performance, cost and features. Contact Innovative Integration with your specific OEM requirements.

Application Information

Application Note: "Multi-channel Software Digital Radio Design Using MATLAB" shows using the UWB with Quadia for a 40 channel receiver.